09/855,660

Docket: XA-9472

Supplemental Application Data Sheet

Application Information

Application Number:: 09/855,660

Filing Date:: 05/16/2001

Application Type:: Regular

Subject Matter:: Utility

Suggested Classification:: 326-121

Suggested Group Art Unit:: 2819

CD-ROM or CD-R? None

Title:: SEMICONDUCTOR INTEGRATED CIRCUIT

HAVING HIGH-SPEED AND LOW-POWER LOGIC

GATES WITH COMMON TRANSISTOR

SUBSTRATE POTENTIALS, AND DESIGN DATA

RECORDING MEDIUM THEREFOR

Attorney Docket Number:: XA-9472

Request for Early Publication?:: No

Request for Non-Publication?:: No

Suggested Drawing Figure:: 1

Total Drawing Sheets:: 22

Small Entity:: No

Petition included?:: No

Secrecy Order in Parent Appl.?:: No

Applicant Information

Applicant Authority type:: Inventor

Primary Citizenship Country:: Japan

Status:: Full Capacity

Given Name:: Yasuhisa

Middle Name::

Family Name:: Shimazaki

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City of Residence::

Richmond

State or Province of Residence::

California

Country of Residence::

United States

Street of mailing address::

c/o Hitachi, Ltd.,12th Floor, Marunouchi Center

Bldg., 6-1, Marunouchi 1-chome, Chiyoda-ku

City of mailing address::

<u>Tokyo</u>

State or Province of mailing address::

Country of mailing address::

<u>Japan</u>

Applicant Authority type::

Inventor

Primary Citizenship Country::

Japan

Status::

Full Capacity
Motoi

Given Name::

Middle Name:: Family Name::

Ichihashi

City of Residence::

Tachikawa

State or Province of Residence::

Country of Residence::

Japan

Street of mailing address::

c/o Hitachi, Ltd.,12th Floor, Marunouchi Center

Bldg., 6-1, Marunouchi 1-chome, Chiyoda-ku

City of mailing address::

Tokyo

State or Province of mailing address::

Country of mailing address::

<u>Japan</u>

Correspondence Informatio	Corres	pondence	Information
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Correspondence Customer Number:: 181

Name:: Mitchell-W. Shapiro

Street of mailing address:: Miles & Stockbridge P.G.

1751 Pinnacle Drive, Suite 500

City of mailing address:: McLean

State of Province of mailing address:: Virginia

Postal or Zip Code of mailing address:: 22102

Telephone:: (703) 903-9000

Fax::

Representative Information

Representative Customer Number::	<u>181</u>

Representative Designation::	Registration number::	Name::
Primary	31,568	Mitchell W. Shapiro

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application			

Foreign Priority Information

Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2000-152732	05/19/2000	Yes

Assignee Information

Assignee Name::

Renesas Technology, Corp.

Street of Mailing address::

4-1, MARUNOUCHI 2-CHOME

Chiyoda-ku

City of Mailing address::

Tokyo

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State or Province of mailing address::

Country of mailing address::

Japan

Postal or Zip Code of Mailing address::